Hao Zheng

Contact Information

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University of South Florida
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Education

Ph.D. in **Electrical Engineering** 1998 – 2001
University of Utah, Salt Lake City, UT

M.S. in **Electrical Engineering** 1996 – 1998
University of Utah, Salt Lake City, UT

B.S. in **Electrical Engineering** 1989 – 1993
Northwestern Polytechnic University, Xi'an, China

Professional Experience

Visiting Faculty, Strategic CAD Lab Summer 2014
Intel, Hillsboro, Oregon

Associate Professor, the Department of Computer Science and Engineering 2010− present
University of South Florida, Tampa, FL

Assistant Professor, the Department of Computer Science and Engineering 2004− 2010
University of South Florida, Tampa, FL

Research Scientist, ASIC Design Group 2001 – 2004
IBM Microelectronics Division, Burlington, VT

Research Assistant, the Department of Electrical and Computer Engineering 1996 – 2001
University of Utah, Salt Lake City, UT

Electronics Engineer, Air China 1993 – 1996
Beijing, China

Research Interests

- Verification and validation of computing systems including software, hardware, networks, etc.
- Formal methods and algorithms for efficient and effective verification and validation
- Modeling, analysis and verification of embedded/cyber-physical systems
- Modeling and analysis of biological systems
- Parallel/distributed computing
- High-performance computing

Awards and Honors

- Best Paper Award, the 21st International SPIN Symposium of Model Checking of Software, 2014.
- USF Graduate School Recognition for Excellence in Mentorship at Master's level for Ryan Mabry, 2007 Outstanding Thesis Award recipient.
- USF Outstanding Research Achievement Award, 2007.
- NSF Faculty Early Career Development (CAREER) Award, 2006.

Research Funding

- H. Zheng (PI), a gift for post-si validation research, **Intel**, $1/2016 - 12/2016$, $\$30,000$.
- H. Zheng (PI), a grant for post-si validation research, **Intel**, $1/2016 - 12/2016$, $\$30,000$.
- H. Zheng (PI), REU supplement grant, **National Science Foundation**, $8/2010 - 7/2011$, $\$12,000$.
- H. Zheng (Lead PI), C. Myers (PI), "CPS:Small:Collaborative Research: Methods and Tools for the Verification of Cyber-Physical Systems", **National Science Foundation**, $9/2009 - 8/2012$, $\$530,000$.
- H. Zheng, "CAREER: Methodologies and Tools for Large Scale Real-Time Concurrent System Verification", **National Science Foundation** CCF-0546492, $3/06 - 2/2011$, $\$400,000$.
- S. Bhanja (PI), V. Jain (co-PI), N. Ranganathan (co-PI), S. Katkoori (co-PI), H. Zheng (co-PI), "CRI: Infrastructure acquisition for sub-100 nano VLSI research", **National Science Foundation** CNS-0551621, $3/2006 - 2/2007$, $\$215,023$,

Publications

Refereed Journal Articles

9. H. Zheng, Z. Zhang, C. J. Myers, E. Rodriguez, and Y. Zhang, "Compositional model checking of concurrent systems," *IEEE Transactions on Computers*, vol. 64, pp. 1607–1621, June 2015
8. H. Zheng and Y. Zhang, "Local state space analysis leads to better partial order reduction," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 33, no. 6, pp. 839–852, 2014
7. H. Zheng, H. Yao, and T. Yoneda, "Modular model checking of large asynchronous designs with efficient abstraction refinement," *IEEE Trans. Comput.*, vol. 59, pp. 561–573, Apr. 2010
6. H. Zheng, "Compositional reachability analysis for efficient modular verification of asynchronous designs," *Trans. Comp.-Aided Des. Integ. Cir. Sys.*, vol. 29, pp. 329–340, Mar. 2010
5. H. Yao and H. Zheng, "Automated interface refinement for compositional verification," *Trans. Comp.-Aided Des. Integ. Cir. Sys.*, vol. 28, pp. 433–446, Mar. 2009
4. H. Zheng, J. Ahrens, and T. Xia, "A compositional method with failure-preserving abstraction for asynchronous design verification," *Trans. Comp.-Aided Des. Integ. Cir. Sys.*, vol. 27, pp. 1343–1347, July 2008
3. T. Xia and H. Zheng, "Timing jitter characterization for mixed-signal production test using the interpolation algorithm," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 1014–1023, 2007
2. H. Zheng, C. J. Myers, D. Walter, S. Little, and T. Yoneda, "Verification of timed circuits with failure-directed abstractions," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 25, no. 3, pp. 403–412, 2006
1. H. Zheng, E. Mercer, and C. J. Myers, "Modular verification of timed circuits using automatic abstraction," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 22, no. 9, pp. 1138–1153, 2003

Refereed Conference/Workshop Papers

23. H. Zheng, Y. Cao, S. Ray, and J. Yang, "Protocol-guided analysis of post-silicon traces under limited observability," in *2016 17th International Symposium on Quality Electronic Design (ISQED)*, pp. 301–306, March 2016
22. H. Zheng, "Local state space construction for compositional verification of concurrent systems," in *Proceedings of the 2014 International SPIN Symposium on Model Checking of Software*, SPIN 2014, (New York, NY, USA), pp. 11–19, ACM, 2014
21. P. Hou and H. Zheng, "Quantified differential temporal dynamic logic for verifying properties of distributed hybrid systems," in *LFCS*, pp. 234–251, 2013
20. Y. Zhang, E. Rodriguez, H. Zheng, and C. Myers, "An improvement in partial order reduction using behavioral analysis," in *VLSI (ISVLSI), 2012 IEEE Computer Society Annual Symposium on*, pp. 100–107, Aug 2012
19. C. J. Myers, J. Wu, Z. Zhang, H. Zheng, and Y. Zhang, "Poster abstract: Methods and tools for verification of cyber-physical systems," in *ICCPS*, p. 232, 2012
18. H. Zheng, A. Price, and C. Myers, "Using decision diagrams to compactly represent the state space for explicit model checking," in *2012 IEEE International High Level Design Validation and Test Workshop (HLDVT)*, vol. 0, (Los Alamitos, CA, USA), pp. 17–24, IEEE Computer Society, 2012
17. H. Zheng, E. Rodriguez, Y. Zhang, and C. Myers, "A compositional minimization approach for large asynchronous design verification," in *Proceedings of the 19th International Conference on Model Checking Software*, SPIN'12, pp. 62–79, Springer-Verlag, 2012
16. Y. Zhang, E. Rodriguez, H. Zheng, and C. J. Myers, "A behavioral analysis approach for efficient partial order reduction," in *HASE*, pp. 49–56, 2011
15. H. Yao, H. Zheng, and C. J. Myers, "State space reductions for scalable verification of asynchronous designs," in *HLDVT*, pp. 17–24, 2010
14. N. Donataccio and H. Zheng, "An improvement in decomposed reachability analysis for symbolic model checking," in *High Level Design Validation and Test Workshop (HLDVT), 2010 IEEE International*, pp. 50–57, June 2010
13. R. A. Thacker, K. R. Jones, C. J. Myers, and H. Zheng, "Automatic abstraction for verification of cyber-physical systems," in *Proceedings of the 1st ACM/IEEE International Conference on Cyber-Physical Systems*, ICCPS '10, (New York, NY, USA), pp. 12–21, ACM, 2010
12. H. Zheng, "A coordinated reachability analysis method for modular verification of asynchronous designs," in *High Level Design Validation and Test Workshop, 2009. HLDVT 2009. IEEE International*, pp. 130–137, Nov 2009
11. H. Zheng, H. Yao, and T. Yoneda, "Synchronization-based abstraction refinement for modular verification of asynchronous designs," in *Proceedings of the 2009 IEEE Computer Society Annual Symposium on VLSI*, ISVLSI '09, (Washington, DC, USA), pp. 175–180, IEEE Computer Society, 2009
10. D. Mu, T. Xia, and H. Zheng, "Data dependent jitter characterization based on fourier analysis," in *Defect and Fault Tolerance in VLSI Systems, 2006. DFT '06. 21st IEEE International Symposium on*, pp. 534–544, Oct 2006
9. T. Xia, H. Zheng, J. Li, and A. Ginawi, "Self-refereed on-chip jitter measurement circuit using vernier oscillators," in *VLSI, 2005. Proceedings. IEEE Computer Society Annual Symposium on*, pp. 218–223, May 2005
8. T. Xia, P. Song, and H. Zheng, "Characterizing the vco jitter due to the digital simultaneous switching noise," in *Proceedings of the 15th ACM Great Lakes Symposium on VLSI*, GLSVLSI '05, (New York, NY, USA), pp. 70–73, ACM, 2005

7. H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, "Verification of timed circuits with failure directed abstractions," in *Computer Design, 2003. Proceedings. 21st International Conference on*, pp. 28–35, Oct 2003
6. E. G. Mercer, C. J. Myers, T. Yoneda, and H. Zheng, "Modular synthesis of timed circuits using partial orders on lpns," in *In Electronic Notes in Theoretical Computer Science (April 2002), U. Nestmann and*, 2002
5. H. Zheng, E. Mercer, and C. Myers, "Automatic abstraction for verification of timed circuits and systems?," in *Computer Aided Verification* (G. Berry, H. Comon, and A. Finkel, eds.), vol. 2102 of *Lecture Notes in Computer Science*, pp. 182–193, Springer Berlin Heidelberg, 2001
4. C. Myers, W. Belluomini, K. Killpack, E. Mercer, E. Peskin, and H. Zheng, "Timed circuits: a new paradigm for high-speed design," in *Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001. Asia and South Pacific*, pp. 335–340, 2001
3. H. Zheng and C. Myers, "Automatic abstraction for synthesis and verification of deterministic timed systems. in collection of papers from tau?00 available from http://www.async.ece.utah.edu," in *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, 2000
2. B. Bachman, H. Zheng, and C. Myers, "Architectural synthesis of timed asynchronous systems," in *Computer Design, 1999. (ICCD '99) International Conference on*, pp. 354–363, 1999
1. C. Myers and H. Zheng, "An asynchronous implementation of the maxlist algorithm," in *Proceedings of the 1997 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP '97) -Volume 1 - Volume 1*, ICASSP '97, (Washington, DC, USA), pp. 647–, IEEE Computer Society, 1997

Ph.D. Dissertation

- Modular Synthesis and Verification of Timed Circuits Using Automatic Abstraction, University of Utah, 2001.

Teaching

University of South Florida (2004 - present)

- CIS 4930/EEL 6706, Testing and Fault-Tolerance of Digital Systems, Spring 2017
- CIS 4930/6930, Principles of Cyber-Physical Systems, Spring 2014
- CIS 4930/6930, Intro. to Embedded System Design, Spring 2012
- CDA 3103, Computer Organization, Fall 2011, 2012, 2013
- CDA 5416, Computer Logic Design, Fall 2010
- CDA 5416, Intro. to Computer-Aided Verification, Fall 2009, 2013, Spring, 2011
- CIS 4930, Design Automation, Spring, 2009
- CDA 4253, FPGA System Design, Fall 2006, 2008, Spring 2010, 2011.
- CDA 5416/CIS 4930, Intro. to Computer-Aided Verification, Spring, 2008, 2011
- COT 3100, Intro. to Discrete Structures, Fall, 2007, 2011, 2012.
- CIS 4930/CIS 6930, Intro. to Computer-Aided Verification, Spring, 2006, 2007.
- CIS 4930, FPGA Design, Fall, 2004, 2005.
- CIS 6930, Asynchronous Circuit Design, Spring, 2005

Students Advised

Current Students:

- Yuting Cao (Ph.D.) 2014 - present
- Hernan Palombo (Ph.D.) 2013 - present

Former Graduate Students:

- Haiqiong Yao (Ph.D.) 2006 – 2012
- Nicholas Donataccio (Ph.D.) 2008 – 2011
- Yangwei Cai (Ph.D) 2010 – 2011
- Yingying Zhang (M.S.) 2010 – 2013
- Emmanuel Rodriguez (M.S.) 2010 – 2012
- Larry Moore (M.S.) 2010 – 2012
- Andrew Price (M.S.) 2012
- Ryan Mabry (M.S., co-advised with Dr. Nagarajan Ranganathan) 2007
  Recipient of 2007 USF Outstanding Thesis Award
- Jared Ahrens (M.S.) 2007

Former undergraduate Research Students

- **REU Students**
  - Michael Kubacki 2011
  - Emmanuel Rodriguez and Larry Moore 2010
  - Francesco DiNatale and Giuseppe DiNatale 2009
  - Christopher Earl 2007
  - Halam Le 2007
  - Paul Ireif 2006
- **Honors Theses**
  - Christopher Cohoon, 2010
  - Ryan Marby, 2005

Invited Talks

- Intel Corporation, 8/2010, 7/2014
- University of Southern California, Los Angeles, 8/2009
- University of British Columbia, Vancouver, Canada, 6/2009
- Brown University, Providence, RI, 3/2009
- NEC Labs America, Princeton, NJ, 2/2009
- IBM Austin Research Lab, Austin, TX, 2/2009
- University of Florida, Gainsville, FL, 11/2008
- Portland State University, Portland, OR, 11/2008
- University of Utah, Salt Lake City, UT, 8/2007
- Xidian University, Xi'an, PRC, 5/2006

Services

IEEE senior member 2010 - present

Program Committees:

- ISVLSI 2014 (Local Arrangement Chair)
- ICCAD 2013 (ACM SIGDA Student Research Competition)
- HLDVT 2010 (Finance Chair)
- HLDVT 2009
- ISVLSI 2009

Reviewer for:

- National Science Foundation, panelist, 2006, 2015, 2016.
- A proposal from Netherlands Organization for Scientific Research, division Physical Sciences
- **Journals**:
  - ACM Transactions on Embedded Computing Systems
  - Formal Methods in System Design
  - IEEE Transactions on Computers
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
  - IEEE Transactions on Very Large Scale Integration Systems
  - IEEE Transactions on Circuits and Systems
  - ACM Transactions on Design Automation of Electronic Systems
  - Journal of Microprocessors and Microsystems
  - IEE Proceedings of Computers and Digital Techniques
  - Transitions on Information Processing Society of Japan
  - Journal of Zhejiang University - Science A
  - Louisiana Board of Regents RCS proposal
- **Conferences**:
  - 2009 : ISVLSI.
  - 2008 : DATE.
  - 2006 : ISCAS and DAC.
  - 2005 : DAC and GLVLSI.

Services to the University

- Chair, the CSE dept. infrastructure committee, 2014 – present.
- Faculty judge for USF Undergraduate Research Symposium, April, 2009.
- Reviewer for USF College of Engineering CAREER reviewing panel Summer 2008
- Faculty advisor of the IEEE Computer Society USF Chapter 2006 – present
  Won **Best Student Organization of College of Engineering** award (2009) .
- Member of the Undergraduate Committee, CSE Dept., USF 2004 – present