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Education

University of Central Florida, Orlando	Computer Science	Ph.D.	1988
	Dissertation: Hardware Algorithms for Data Compression		
University of Madras, India	Electrical & Electronics	B.E. (Honors)	1983

Work Experience

Since 2007	Distinguished University Professor, Dept. CSE, Uni. South Florida, Tampa
1998-2007	Professor, Dept. CSE, Uni. South Florida, Tampa
1998-1999	Professor, Dept. of EE, Uni. of Texas at El Paso (on courtesy appointment at USF)
1993-1998	Associate Professor, Dept. CSE, Uni. South Florida, Tampa
1988-1993	Assistant Professor, Dept. CSE, Uni. South Florida, Tampa
1984-1988	Graduate Research/Teaching Assistant, Dept. of CS, Uni. of Central Florida, Orlando.
1983-1983	Systems Executive, International Computers Limited (U.K.), Bombay, India. June- Dec.

Research

Research areas include VLSI circuits and systems design, VLSI design automation, computer architecture, low power design, reversible logic, nano-architectures, hardware algorithms, parallel processing, data compression, and VLSI for vision, video, image processing, pattern recognition.

Courses

Undergraduate: Computer Organization and Architecture, CMOS VLSI Design, Embedded Systems

Graduate: Advanced Computer Architecture I, Advanced Computer Architecture II, Parallel Processing, CMOS VLSI Design, VLSI Algorithms and Architectures, Bio-information Processing, Advanced VLSI Systems

Affiliations

Fellow of the IEEE, (S-'81, M-'88, SM-'93, F-'02)
Fellow of the AAAS, 2012
Member of the IEEE Computer and Circuits & Systems Societies, since 1988
Member of the VLSI Society of India, 1988

Honors and Awards

- Fellow of AAAS, for contributions to algorithms and architectures for VLSI systems design, 2012.
- Best Paper Award in Ph.D. Forum of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Amherst, August 2012: H. Thapliyal and N. Ranganathan, Design, Synthesis and Test of Reversible Circuits for Emerging Nanotechnologies", Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), August 2012.
- Honorary Mention for USF Graduate Outstanding Mentor Award, 2011.
- USF Outstanding Undergraduate Teaching Award, 2009.
- IEEE Circuits and Systems Society VLSI Transactions Best Paper Award, 2009 for the paper: V. Mahalingam, N. Ranganathan and J. E. Harlow, Fuzzy Optimization Approach for Gate Sizing in the presence of Process Variations, IEEE Transactions on VLSI Systems, 16(8), Pp. 975-984, Aug. 2008.
- Distinguished Alumnus Award, National Institute of Technology (Regional Engineering College), Trichy, India, 2009.
- Distinguished University Professor Honorific Title and University Gold Medallion Honor, 2007.
- Best Paper Award, ranked 1 out of 360 submissions: N. Hanchate and N. Ranganathan, "A Linear
- Time Algorithm for Wire Sizing with Simultaneous Optimization of Interconnect Delay and Crosstalk Noise", Proc. Intl. Conf. on VLSI Design, Jan 2006.
- Best Paper Award, ranked 1 out of 330 submissions, Intl. Conf. on VLSI Design, Jan 2004, "Gate Sizing and Buffer Insertion Using Economic Models for Power Optimization," co-authored with A. Murugavel.
- Best Paper Award, ranked 1 out of 139 submissions, Intl. Conf. on VLSI Design, 1995, "JAGUAR: A VLSI Chip for JPEG Image Compression Standard," co-authored with M. Kovac.
- Best Paper Award Nominations, ranked within top 6-8 papers based on independent/blind reviews, forwarded to the Best Paper Award Panel, Intl. Conf. on VLSI Design, 1995,98,00,02,04,06.
- Best Paper Award Nomination, ranked within top 6 out of 220 papers, Great Lakes Symposium on VLSI, 2008.
- USF Theodore and Venette Askounes-Ashford Distinguished Scholar Award, 2003.
- SIGMA XI Scientific Honor Society Tampa Chapter Outstanding Faculty Researcher Award, 2004.
- USF President's Award for Faculty Excellence, 2002-03.
- USF Division of Sponsored Research Outstanding Research Achievement Award, 2002.
- Fellow of IEEE, for contributions to algorithms and architectures for VLSI systems design, Jan 2002.
- Editor-In-Chief, IEEE Transactions on VLSI Systems, two terms, Jan 2003 to Jan 2007.
- Certificate of Appreciation (Associate Editor of IEEE Trans. Video Technology), IEEE Circuits & Systems Society, 2000-2002
- Certificate of Appreciation (Associate Editor of IEEE Trans. Circuits & Systems, TCAS-II), IEEE Circuits & Systems Society, 1999.
- Certificate of Appreciation (for service as associate editor of IEEE Transactions on VLSI Systems), From IEEE Circuits and Systems Society, 1997.
- Certificate of Appreciation (for distinguished service in student activities), from IEEE Computer Society, February 1996.
- Outstanding Researcher Award ($1000), 1995, USF College of Engineering.
- IEEE Computer Society Distinguished Visitor Program Speaker, 1995-03.
- Outstanding Young Investigator Award ($1000), 1991-1992, in recognition of research, University of South Florida College of Engineering.

- IEEE Computer Society R. E. Merwin Fellowship Award ($3000), 1987-88, for academic achievement, leadership and service to IEEE Computer Society student chapter at UCF-Orlando.
- Rotary Foundation Graduate Fellowship ($20K), 1984-85, awarded by the Rotary Foundation of the Rotary International, Washington D.C., Dt. 320 - includes four states in S. India and Sri Lanka.
- IEEE Region X Outstanding Student Branch Chairman Award ($500), 1982. Region X includes India, China, Japan, Australia, New Zealand and other Southeast Asian countries.
- IEEE Outstanding Student Award, 1981-82, from IEEE Past-President Dr. James B. Owens for contributions towards IEEE activities as a student.
- Rotary Foundation Youth Merit Award, 1982, as outstanding student of Rotary District 320.
- National Merit Certificate, 1978, from Central Ministry of Education, Govt. of India for 19th rank out of about 250,000 students in the Higher Secondary School State-wide Examinations.
- Isaac Daniel Gold Medal, 1977, outstanding student in Tanjore City, based on academics, sports, quiz and debate teams, 1977.
- Marsh Gold Medal, 1977, awarded by the Union Club of Tanjore for First rank in the Higher Secondary School State-wide Examinations.
- Koil Pillai Good Conduct Certificate and Prize, St. Peter's High School, Tanjore, India, 1977.
- Bible Study Gold Medal, St. Peter's High School, 1977.

Honors and Awards To My Students

- Best Paper Award in Ph.D. Forum- Major Professor for Himanshu Thapliyal, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2012.
- USF Provost's Outstanding Teaching Award- Major Professor for Matthew Morrison, 2012.
- USF Graduate Council Outstanding Dissertation Award- Major Professor for K. Bhattacharya, Architectures and Algorithms for Mitigation of Soft Errors in Nanoscale VLSI Circuits, Dec 2009.
- USF Graduate Council Outstanding Dissertation Award- Major Professor for U. Gupta, Utilitarian Approaches for Multi-Metric Optimization in VLSI Circuit Design and Spatial Clustering, 2008.
- USF Graduate Council Outstanding Thesis Award, Co-Major Professor to R. Mabry, Power Estimation in Asynchronous Circuits Using Petrinets, Aug 2007.
- USF Graduate Council Outstanding Dissertation Award - Major Professor, for A. Murugavel, Power Estimation and Optimization in VLSI Circuits, 2003.
- SIGMA XI Tampa Bay Chapter Outstanding Dissertation Award - Major Professor for A. Murugavel, Power Estimation and Optimization in VLSI Circuits, 2003.
- USF Graduate Council Outstanding Dissertation Award - Major Professor, for R. Chandramouli, Theory and Application of Sequential Detection under Dependence, Jan 1999.
- USF Graduate Council Outstanding Dissertation Award -Major Professor, V. Krishna, High Level Techniques for Power Estimation, Analysis and Optimization, Jan 1999.
- USF Graduate Council Outstanding Dissertation Award - Major Professor, R. Sastry, VLSI Architectures for Pattern Matching and Recognition, Aug 1994.
- SIGMA XI Tampa Bay Chapter Outstanding Dissertation Award - Major Professor, R. Sastry, VLSI Architectures for Pattern Matching and Recognition, Aug 1994.

Professional Activities

- Special Issue on Reversible Computing, Springer Transactions on Computational Science, Guest Editors H. Thapliyal and N. Ranganathan, Dec 2014.
- IEEE Computer Society Fellows Selection Committee, 2013, 2014, 2015.
- Co-organizer, Special Session on "Reversible Computing", 56th International Midwest Symposium on Circuits and systems (IEEE MWSCAS 2013), Columbus, Ohio, August 2013.
- Associate Editor, IEEE Transactions on CAD, 2008-11.
- Associate Editor, IEEE Transactions on Computers, 2008-13.
- Associate Editor, ACM Transactions on Design Automation of Electronic Systems, 2007-2011.
- Steering Committee Member, IEEE Transactions on VLSI Systems, 2007-2012.
- Steering Committee Member, IEEE Transactions on NanoBioScience, 2007-08.
- Editor-in-Chief, IEEE Transactions on VLSI Systems, two terms, 2003-06.
- EIC Search Committee, IEEE Transactions on VLSI Systems, Dec 06.
- Best Paper Awards Panel for IEEE Circuits and Systems Society, 2002-05.
- Outstanding Young Author Award Panel for IEEE CAS Society, 2002-05.
- Steering Committee Chair, IEEE Trans. VLSI Systems, 2001-02.
- Steering Committee Chair, IEEECS Annual Symposium on VLSI (ISVLSI), 2012-2015.
- Steering Committee Member, IEEE Trans. VLSI Systems, 1999-00, 2007-08.
- IEEE Computer Society Technical Committee on VLSI (TCVLSI) Chair, 1997-2001.
- Associate Editor, IEEE Trans. on Circuits & Systems, 1997-99.
- Associate Editor, IEEE Trans. on CAS for Video Technology, 1997-00.
- Associate Editor, IEEE Trans. on VLSI Systems, 1995-1997.
- Associate Editor, Pattern Recognition Journal, 1993-02.
- Editorial Board, International Journal of VLSI Design, since 1994.
- Editor, Special Issue on VLSI, Intl. Jour. of Pattern Recognition & Artificial Intelligence, (9)2, 1995.
- IEEE Computer Society Activities:

– IEEECS Distinguished Visitors Program Speaker, 1995-2001.
– IEEE/ACM CSE Curriculum Task Force (national level), 2004-06.
– Executive Committee Member of IEEECS SAC, 1993-95.
– Executive Member, IEEECS Membership Activities Board MAB, 1996-97.
– Executive Member, IEEECS Educational Activities Board EAB, 1996-97.
– Coordinator, IEEECS intl. student newsletter looking .forward, 1996-1998.
– Faculty Advisor, IEEECS Student Chapter, Uni. of S. Florida, 1990-1998.

- Conferences Organization:

– General Co-chair, IEEE CS Annual Symposium on VLSI, August 2011, 2014.
– Mentor, IEEE CS Annual Symposium on VLSI, July 2012.
– General Co-Chair, IEEECS Annual Symposium on VLSI, May 2009.
– Program Co-Chair, Intl. Conf. on VLSI Design, Jan 2008.
– Design Tools Track Chair, Program Committee, Intl. Symp. Quality of Electronic Design, 2006, 2007, 2008.
– Best Paper Award Panel, ISLPED 2006.
– Best Paper Award Panel, Intl. Conf. on VLSI Design, 2007, 2008.

– Steering Com. Member, Intl. Conf. on VLSI Design, 1992-Present.
– Steering Com. Member, IEEECS Annual Symposium on VLSI, 1992-present.
– Steering Com. Member, Intl. Symp. Quality of Electronic Design, 2000-02.
– General Chair, IEEECS Annual Symposium on VLSI, Tampa, Feb 2005.
– Program Co-Chair, IEEECS Annual Symposium on VLSI, Tampa, Feb 2003.
– Publications Chair and IEEE Liaison, Intl. Conf. on VLSI Design, 2003, 2004, 2006.
– General Chair, IEEECS Annual Workshop on VLSI, Orlando, April 1999.
– General Co-Chair, IEEECS Workshop on VLSI, Orlando, April 1998.
– General Co-Chair, Intl. Conf. on VLSI Design, Madras, Jan 4-7, 1998.
– Publicity Chair, Intl. Workshop on CAMP, Boston, Oct 20-22, 1997.
– Workshop Chair, IEEECS Workshop on VLSI, Orlando, April 1998.
– Program Chair, IEEECS Workshop on VLSI, Clearwater, Nov 3-6, 1996.
– Publicity Chair, Intl. Conf. on VLSI Design, 1992, 1996, 1997.
– General Co-Chair, Intl. Conf. on VLSI Design, New Delhi, Jan 1995.
– Panel Moderator, Intl. Conf. on Parallel Processing, 1995.
– Program Chair, Intl. Conf. on VLSI Design, Calcutta, Jan. 1994.
– IEEE Liaison, Intl. Conf. on VLSI Design, 1993, 1999-2010.
– Local Arrangements Chair, IEEECS VLSI Workshop, Tampa, Feb 2-5, 1992.
– Best Paper Award Panel, Intl. Conf. VLSI Design, 1996, 99, 2001.
• Conferences Program Committee Member:
– Intl. Conference on Parallel Processing, ICPP, August 15-17, 1995;
– Intl. Symposium on Parallel and Distributed Processing, SPDP, 1995.
– Intl. Conf. on High Performance Computing, ICHPC, 1995-1997.
– Intl. Parallel Processing Symposium, IPPS, Santa Barbara, April 1995.
– Intl. Conf. on Computer Design, ICCD, 1994-1997, 1999, 2002-06,2009-2010.
– Intl. Conference on VLSI Design, 1993-2011.
– IEEE Computer Society Annual Workshop on VLSI, 1992-1999, 2002.
– IEEECS Intl. Symposium on VLSI, 2003-09.
– IEEE Great Lakes Symposium on VLSI, GLSVLSI, 1998, 2002, 2010.
– Intl. Workshop on Asynchronous Systems, ASYNC, 1999, 2000.
– Intl. Workshop on Design, Test and Applications, WDTA99, Croatia.
– Intl. Conf. Parallel & Distr. Proc. Techniques & Applications., PDPTA99.
– Microelectronic Systems Education Conference, 1999, 2000-05.
– Intl. Sym. on Quality of Electronic Design, 2000-01.
– Intl. Sym. on Low Power Electronics and Design (ISLPED), 2004-08.
– Intl. Sym. on Circuits and Systems (ISCAS), 2006-2010.
– Intl. Conference on Computer Aided Design (ICCAD), 2006, 2007.
– Intl. Conference on Computer Architectures for Machine Perception, 1997, 2000, 2003, 2006.
– Intl. Symposium on Electronic Design (ISED), 2010.
• Conferences Session Chair:
– VLSI Algorithms, Intl. Conf. on VLSI Design, New Delhi, Jan 4-8, 1991.
– Layout, Fifth Intl. Conf. on VLSI Design, Bangalore, Jan 4-8, 1992.
– Special Purpose Architectures, Sixth IPPS, Beverly Hills, Mar 23-26, 1992.
– VLSI for Machine Vision, SPIE Conf. on Applications of AI X: Machine Vision and Robotics,

Orlando, April 20-24, 1992.
– DSP, Intl. Conf. on VLSI Design, Bombay, Jan 4-7, 1993.
– Computer Arithmetic, Intl. Conf. on Computer Design, Boston, Oct 1994.
– Architecture/Design, Great Lakes Symposium on VLSI, Buffalo, Mar 1995.
– Special Purpose Architectures, 9th IPPS, Santa Barbara, April 1995.
– Algorithms on Networks I, ICPP, Wisconsin, Aug 1995.
– Arithmetic Modules, Intl. Conf. on Computer Design, Austin, Oct 1995.
– Image Processing, ICHPC, High Performance Computing, Dec 27-30, 1995.
– Arithmetic Circuits, ICCD, Austin, Oct. 7-9, 1996.
– VLSI, Computer Arch. for Machine Perception, Boston, Oct 20-22, 1997.
– VLSI Architectures I, Intl. Conf. on VLSI Design, 2002.
– Low Power, IEEE Symposium on Low Power Electronics and Design, 2002.
– Low Power, International Conference on VLSI Design, 2004.
– VLSI Circuit Design, GLSVLSI, 2008.
– Power Optimization, ISLPED, 2008.

• Review Work:

National Science Foundation SBIR Panel, 2007.
National Science Foundation ITR Panel, 2003, 2004.
National Science Foundation Design Automation Panel, 2003, 2006.
VLSI RISC Architectures and Organization by S. Furber, book review appeared in Journal of Computer Systems Science and Engineering, 6(1), Jan 1991;
Parallel and Distributed Computing Handbook by A. Zomaya, book review appeared in IEEE Concurrency Magazine, 5(3), Sept 1997;

• Reviewer for journals:

IEEE Trans. on Computers, VLSI Systems, Computer Aided Design, Circuits and Systems, SMC, Parallel and Distributed Processing, CSVT, Signal Processing and PAMI, IEEE Computer, Proc. of IEEE, IEEE Micro, Machine Vision and Applications Journal, Journal of Parallel and Distributed Computing, IEEE Design and Test, Pattern Recognition Journal, Pattern Recognition Letters.

• Reviewer for Conferences:

IEEE Robotics and Automation, IROS, Phoenix Conf. on Computers and Comm., ICPP, ICCD, ISCAS, ICCAD, MSE, ISVLSI, ISQED, ISLPED, IPPS, SPDP, MPPS, VLSI Design, CAMP, and DAC (for many years).

• Service at USF:

IEEE Computer Society Fellows Selection Committee, 2012; University Recommending Committee for Distinguished University Professor, (2012-15); Faculty Liaison to USF Board of Trustees ACE Group, (2011-14); Provost's Tenure and Promotion Guidelines Committee, 2010-11; Faculty search committee chair (2003-2005, CSE Dept hired 6 tenure track and 5 non-tenure track faculty); Faculty search committee member (2000-05,07); CSE chair search committee (2003-04); EE chair search committee (2003-04); CSE graduate program committee (1989-98,99-03); Graduate/Ph.D. Qualifiers Examination Committee (1988-98,99-07); Faculty Governance Committee for College of Engineering(1999-2005); NNRC advisory committee (2004-06;2010); CMR executive committee (1994-98); CSE library representative (1993-1997); CSE awards committee chair (1994-95); CSE infrastructure committee chair (2006-07); CSE strategic planning committee (2004-05); USF graduate council awards committee (2003-04); CSE undergraduate curriculum committee (1999-03).

Grants and Contracts

- ”VLSI Clock Control Mechanism: Phase II”, $42,696, Florida High Tech Corridor ($21,348) and EWI Corporation ($21,348 and $21,348 in-kind), 2010-12.
- ”VLSI Clock Control Mechanism: Phase I”, $21,348, East West Innovation Corporation and Florida High Tech Corridor, 2009-10.
- ”Multi-metric Optimization Considering Process Variations in Deep Submicron and Nanometer Design”, $315K, PI, Semiconductor Research Corporation, ($270K from SRC and $45K from USF), 2007-2010.
- ”The Tessera Project: A New Image Registration Algorithm and Its FPGA Realization for UAV”, $48,121, Tessera, PI with Co-PI Dr. R. Murphy, 2007.
- ”CRI: Infrastructure Acquisition for Sub-100 Nano-VLSI Research”, $215,023, National Science Foundation, Co-PI with PI S. Bhanja, 2006.
- ”Dynamic Resource Allocation for Urban Multi-Event Crisis Management”, $179,179 ($59,179 from I-4 High Tech Corridor Initiative and $120K from Aeolus Systems), 2004.
- ”A Game Theoretic Framework for VLSI Design Automation”, $40K, Semiconductor Research Corporation (SRC), 2004.
- ”SKINS: Sensory Knowledge-Based Interface Science - IGERT”, $3,440,280, National Science Foundation, Co-PI and Project Co-Director, 2003-2008.
- ”IEEE Transactions on VLSI Systems EIC Funding” from IEEE, $130K, 2003-06.
- ”Dynamic Task Scheduling in Heterogenous Computing Systems”, $143K ($105K from Tandel Systems Inc. and $38K from I-4 High Tech Corridor Initiative), 2002-03.
- ”Mapping Applications to Networked Heterogenous Computing Systems”, $102K ($68K from Honeywell and $34K from I-4 High Tech Corridor Initiative), 2001-02.
- ”Switching Activity Estimation Using Bayesian Networks”, $195K, National Science Foundation, 2001-2004.
- ”Task Assignment and Scheduling for Heterogenous Computing Systems”, $93,244 ($65K from Honeywell and $28,244 from I-4 High Tech Corridor Initiative), 2000-01.
- ”Design of System/RT Level Power Estimator Tool”, $27,000 ($15K from Honeywell, Clearwater and $12K from I-4 High Tech Corridor Initiative), 1999-00.
- ”Introducing Design into Undergraduate Computer Sci. and Eng. Curriculum”, $659,734 ($286,210-USF), National Science Foundation, 1995-1999, Co-PI with P.M. Maurer, L.K. John.
- ”Hardware and Software Design for Image Reconstruction”, $98,165, jointly with Dynacs Engineering
- Co., NASA TRP RAMP Program, 1996-1997.
- ”VLSI Architectures for PatternMatching and Recognition”,$196,968 ($138,190 from NSF and $58,778 USF matching), MIPS 9407034, 1994-1998.
- ”Hardware and Software Design for Real-Time Multimedia Applications,” jointly with Dynacs Engineering Co., NASA TRP RAMP Program, $116,604, 1995-1996.
- ”VLSI Hardware for Image Processing,” Dynax Engineering Inc., $25,755, 1996-97.
- ”Hardware/Software Design for High Performance Computing in Simulation Environments,” jointly with Dynacs Engineering Co., NASA TRP RAMP Program, $97,349, 1994-95.
- ”Parallel/VLSI Algorithms for Data Compression,” $123,438, Florida High Technology and Industry Council, 1990-1995.
- ”Software Development and Testing,” $6,875 from Dynax Engineering Inc., 1994.

- ”Computer Vision Hardware/Algorithms”, $11,020, Insight Control Systems, 1995.
- ”Graduate Student Support”, $13,236, Danka Industries Inc., 1995-96.
- ”MOSIS Fabrication of VLSI design Projects,” $32,800, NSF-DARPA Program, 1990-94.
- ”Reduced Cycle Nonlinear Multi-function Chips,” $264,927 ($171,000 from National Science Foundation, $93,927-USF) 1991-93, Co-PI with V. Jain, D.L. Landis, MIP-9103286.
- ”VLSI Algorithms and Architectures for Image Processing,”$100,160 ($70,000 from National Science Foundation, 1990-1993 ($30,160 USF matching) - MIP-9010358.
- ”VLSI Hardware for Performance Improvement in a Relational Database System,” $8000, College of Engineering, University of South Florida, 1989-91.
- ”VLSI Algorithms for Data Compression,” $3000, USF Sponsored Research, 1989.

Books

1. VLSI Algorithms and Architectures: Fundamentals, edited by N. Ranganathan, IEEE Computer Society Press, June 1993.
2. VLSI Algorithms and Architectures: Advanced Concepts, edited by N. Ranganathan, IEEE Computer Society Press, June 1993.
3. VLSI for Pattern Recognition and Artificial Intelligence, edited by N. Ranganathan, World Scientific Publishing Co., April 1995.
4. Low Power High Level Synthesis for Nanoscale CMOS Circuits, S. Mohanty, N. Ranganathan, E. Kougianos and P. Patra, Springer, Jan 2008.

Book Chapters

1. N. Ranganathan and S. Henriques, ”High Speed VLSI Designs for Lempel-Ziv based Data Compression”, IEEETCAS-II paper included in ”High Performance VLSI Signal Processing - Innovative Architectures and Algorithms Vol I & II” by K.J. Ray Liu and K. Yao, IEEE Press, 1997.
2. N. Ranganathan and R. Venkataramana, ”Integrated Circuits”, invited article in 24-Volume Encyclopedia of Electrical Engineering, published by John Wiley and Sons, 1998.
3. M. Patel and N. Ranganathan, ”A VLSI System for Intelligent Decision Making”, invited chapter in ”Neural Networks and Systolic Arrays”,by D. Zhang and S.K. Pal, World Scientific Publishers, 2002.
4. S.Bhanja and N. Ranganathan, Hardware Implementation of Data Compression, in Lossless Compression Handbook, edited by K. Sayood, ISBN # 0-12-620861-1, Academic Press, 2003.
5. H. Thapliyal, N. Ranganathan, and S. Kotiyal Book Chapter Title: Reversible Logic Based Design and Test of Field Coupled Nanocomputing Circuits in the Book, Springer Lecture Notes on Computer Science State-of-the-Art-Survey Series Special Volume on Field-Coupled Nanocomputing, Dec 2013.

U.S.Patents

1. Conservative Logic Gate for Design of Quantum Dot Cellular Automata Circuits, N. Ranganathan and H. Thapliyal, U.S. Patent No. 7,880496, February 2011.
2. RADJAM: Methodology and Apparatus for Reduction of Soft Errors in Logic Circuits, N. Ranganathan and K. Bhattacharya, U.S. Patent No. 7,804,320 B2, Sept 28, 2010.
3. Method and Apparatus for Reducing Leakage in CMOS VLSI Circuits, U.S. Patent No. 7,256,608, Aug 2007.
4. High Speed VLSI Hardware for Lempel-Ziv Based Data Compression, U.S. Patent 5,179,378, Dec 1993.
5. Structure and Method for Dynamic Scene Analysis, U.S. Patent 5,604,821 Jan 1996.
6. VLSI Architectures for Polygon Recognition, U.S. Patent 5,535,292, July 1996, licensed by Intellectual Ventures Holding 10 LLC, 2007.
7. A VLSI Circuit Structure for Determining the Edit Distance Between Strings, U.S. Patent 5,553,272,, Sept 1996.
8. A VLSI Circuit Structure for Implementing JPEG Image Compression Standard, U.S. Patent 5,659,362, Aug 1997 and International Patent allowed.
9. 13B129_M. Morrison and N. Ranganathan | Title: Design of Adiabatic Dynamic Differential Logic for DPA-Resistant Secure Integrated Circuits; Patent submitted.
10. AMD-130071_ S. Roy, Y. Wang and N. Ranganathan | Title: Run-time Power-gating in Caches of GPUs for Leakage Energy Savings; AMD has indicated interest to submit the patent.

Tutorials

1. H.Thapliyal and N. Ranganathan, "Reversible Logic: Basics, Prospects in Emerging Nanotechnologies and Challenges in Future", Tutorial at 55th International Midwest Symposium on Circuits and systems (IEEE MWSCAS 2012), Boise, Idaho, August 5-8, 2012
2. H.Thapliyal and N. Ranganathan, "Reversible Logic: Fundamentals and Applications in Ultra-Low Power, Fault Testing and Emerging Nanotechnologies, and Challenges in Future", Tutorial at 25th International Conference on VLSI Design (VLSI Design), Hyderabad, India, Jan 2012, pp. 13-15.
3. N. Ranganathan, "Special Purpose VLSI Architectures", Invited Full day Tutorial at KAIST, South Korea, May 2011.
4. N. Ranganathan, "Impact of VLSI Technology on Architecture", Invited Full day Tutorial at KAIST, South Korea, May 2011.
5. N. Ranganathan, "Game Theory in VLSI Design", Invited Full-day Tutorial at KAIST, South Korea, May 2011.

Journal Editorial Articles

1. N. Ranganathan, Editorial: A Reflection on the TVLSI Editorial Process and the Announcement of a New Editor-In-Chief, IEEE Transactions on VLSI Systems, 15(1), Pp. 1-4, Jan 2007.
2. N. Ranganathan, Editorial: New Members of the Editorial Board, IEEE Transactions on VLSI Systems, 14(12), 1293-1294, Dec 2006.
3. N. Ranganathan, Editorial Appointments for 2005-2006 Term, IEEE Transactions on VLSI Systems, 13(7), Pp. 773-782, July 2005.
4. N. Ranganathan, Editorial: The Responsibility of Reviewers, IEEE Transactions on VLSI Systems, 12(12), pp. 1261-1262, Dec 2004.
5. N. Ranganathan, Editorial: Another Step in the Right Direction for TVLSI, IEEE Transactions on VLSI Systems, 12(7), Pp. 673, July 2004.
6. N. Ranganathan, Editorial, IEEE Transactions on VLSI systems, 12(1), Pp. 1-11, Jan 2004.

Journal Publications

1. W-Y. Tsai, X. Li, M. Jerry, B. Xie, N. Shukla, H. Liu, N. Chandramoorthy, M. Cotter, A. Raychowdhury, D. M. Chiarulli, S.P. Levitan, , S. Datta, J. Sampson, N. Ranganathan, and V. Narayanan, "Enabling New Computation Paradigms with HyperFET - an Emerging Device", To appear in IEEE Transactions on Multi-Scale Computing Systems, 2015.
2. S.Kotiyal, H. Thapliyal and N. Ranganathan," Reversible Logic Based Multiplication Computing Unit using Binary Tree Data Structure", Accepted in Journal of Supercomputing, March 2015.
3. M Morrison and N. Ranganathan, "Synthesis of Dual-Rail Adiabatic Logic for Low Power Security Applications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.33, no.7, pp.975,988, July 2014.
4. S. Kotiyal, H. Thapliyal and N. Ranganathan, "A New Class of All Optical Reversible NOR Gates and Their MZI Based Design" Microelectronics Journal, Volume 45 (6), June 2014, Pages 825-834.
5. S. Kotiyal, H. Thapliyal and N. Ranganathan, "Design of Reversible Adder-Subtractor and Its Mapping In Optical Computing Domain", Transactions on Computational Sciences Journal, XXIV, Springer, Lecture Notes in Computer Science, 2014, Vol. 8911, Pages 37-55.
6. H. Thapliyal, N. Ranganathan and S.Kotiyal, "Reversible Logic Based Design and Test of Field Coupled Nanocomputing Circuits", Springer Lecture Notes on Computer Science State-of the-Art-Survey Series Special Volume on Field-Coupled Nanocomputing, 2014, pp. 133-172.
7. M. Morrison, N. Ranganathan, and J. Ligatti, .Design of Adiabatic Dynamic Differential Logic for DPA-Resistant Secure Integrated Circuits, IEEE Transactions on Very Large Scale Integration, 2014.
8. H. Thapliyal, N. Ranganathan and S. Kotiyal,"Design of Testable Reversible Sequential Circuits", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume 21 (7), 2013, Pages 1201-1209.
9. R. Hyman, N. Ranganathan, T. Bingel and D. Tran Vo, "A Clock Control Strategy for Peak Power and RMS Current Reduction Using Path Clustering", IEEE Transactions on VLSI Systems, 21 (2), Pages 259-269, February 2013.
10. H. Thapliyal and N. Ranganathan,"Design of Efficient Reversible Logic Based Binary and BCD Adder Circuits", ACM Journal of Emerging Technologies in Computing Systems, 9 (3), Sept., 2013.

11. V. Mahalingam, N. Ranganathan and R. Hyman,"Dynamic Clock Stretching for Variation Compensation in VLSI Circuit Design," ACM Journal of Emerging Technologies in Computing Systems, 8 (3), August 2012.
12. S. Roy, N. Ranganathan, and S. Katkoori. "State Retentive Power Gating of Register Files in Multi-core Processors", IEEE Transactions on Computers, 60(11), Nov 2011, Pp. 1547-1560.
13. R. Hyman, K. Bhattacharya and N. Ranganathan, "Redundancy Mining for Soft Error Detection in Multi-core Processors", IEEE Transactions on Computers, 60(8), August 2011, Pp. 1114-1125.
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177. K. Hughes, A. Tokuta and N. Ranganathan,”TRULLA : An Algorithm for Path Planning Among Weighted Regions by Localized Propagations,” Proc. Fifth Intl. Conference on Intelligent Robots and Systems, Iros’, Raleigh, North Carolina, July 7-10, 1992.
178. A. Mukherjee, J. Flieder and N. Ranganathan, ”MARVLE: A VLSI Chip for Variable Length Encoding and Decoding,” Proc. IEEE Intl. Conference on Comuter Design ICCD , Cambridge, Massachusetts, October 11-14, pp. 170-173, 1992.
179. M. Patel, P. McCabe and N. Ranganathan, ”SIBA: A VLSI Chip for Image Processing,” Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, August 1992, Vol. IV, pp. 15-18.
180. V.K. Sundaresan, S. Nichani, N. Ranganathan and R. Sankar, ”A VLSI Hardware Accelerator for Dynamic Time Warping,” Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, pp. 27-30, Vol. IV, August 1992.
181. R. Venkatesan, R. Sastry and N. Ranganathan, ”A VLSI Architecture for Hierarchical Scene Matching,” Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, pp. 214-217, August 1992.

182. K. Namuduri, R. Mehrotra and N. Ranganathan, ”Edge Detection using Gabor Filters,” Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, Vol. III, pp. 729-733, August 1992.
183. Ranganathan and K. R. Balaji, ”A VLSI Chip for Attribute-based Relational Databases,” Proc. International Conference on Information Systems and Management of Data, CISMOD, Bangalore, India, pp. 77-92, July 21-23, 1992.
184. M. Kovac, N. Ranganathan and M. Varanasi, ”A Systolic Algorithm and Architecture for Galois Field Arithmetic,” Proc. of Intl. Parallel Processing Symposium, Beverly Hills, California, pp. 283-288, March 23-25, 1992.
185. N. Ranganathan, S. Kurji and R. Mehrotra, ” A CMOS VLSI Chip for Motion Detection,” Proc. of Intl. Conference on VLSI Design, Bangalore, India, pp. 209-214, Jan 1992.
186. N. Ranganathan, Patrick McCabe and M. Patel, ”A Programmable 2-dimensional Systolic Processor using 4-bit Processing Elements for Image Processing,” Proc. of Intl. Conference on VLSI Design, Bangalore, India, pp. 215-220, Jan 1992.
187. S. Nichani and N. Ranganathan,”Design of a High Speed VLSI Chip for Scale Space Computation,” Proc. of SPIE Conference on Applications of Artificial Intelligence X : Machine Vision and Robotics, Orlando, April 20-24, 1992.
188. N. Ranganathan, R. Mehrotra and S. Subramaniam ”A High Speed Systolic Architecture for Labeling Connected Components in an Image,”Proc. IEEE International Symposium on Parallel and Distributed Processing, Dallas, Texas, pp. 818-825, December 1-5, 1991.
189. K. Chaudhury, R. Mehrotra and N. Ranganathan, ”A Parallel Algorithm for 3-D Point Pattern Matching,” Proc. IEEE Intl. Conference on Systems, Man and Cybernetics, Charlottesville, Virginia, pp. 105-111, Oct. 13-16, 1991.
190. N. Ranganathan and S. Henriques,”A Systolic Architecture for LZ-based Decompression,” Proc. of Data Compression Conference, Snowbird, Utah, pp. 450-451, April 8-11, 1991.
191. N. Ranganathan and S. Henriques,”A Systolic VLSI Chip for Data Compression,” Proc. IEEE International Symposium on VLSI Design, New Delhi, pp. 310-311, Jan 4-8, 1991.
192. N. Ranganathan, K. Namuduri and R. Mehrotra, ”An Architecture to Implement Multiresolution,” Proc. of IEEE Intl. Conf. on ASSP, Toronto, Canada, May 14-17, pp. 1157-1160, 1991.
193. S. Henriques and N. Ranganathan,”A Parallel Architecture for LZ-based Data Compression,” Proc. IEEE Intl. Symposium on Parallel and Distributed Processing, Dallas, pp. 262-266, Dec 9-13, 1990.
194. S. Nichani and N. Ranganathan, ”SAP: Design of a Systolic Array Processor for Computations in Vision,” Proc. IEEE International Conference on Computer Design, ICCD ’90 , Cambridge, MA, pp. 315-318, September 17-19, 1990.
195. K. Namuduri, R. Mehrotra and N. Ranganathan, ”Fast Spatiotemporal Filters,” Proc. 10th Intl. Conference on Pattern Recognition, Atlantic City, pp. 479-483, June 16-21, 1990.
196. N. Ranganathan and R. Mehrotra ”A VLSI Architecture for Dynamic Scene Analysis,” Proc. 10th Intl. Conf.on Pattern Recognition, Atlantic City, pp. 506-508, June 16-21, 1990.
197. N. Ranganathan and H. N. Srinidhi,”Effect of Data Compression Hardware on the Performance of a Relational Database Machine,” Proc. IEEE Intl. Conf. on Parallel Architectures & Databases (PARBASE ’90), Miami, pp.144-146, March 7-9, 1990.
198. Ranganathan, S. Nichani and R. Mehrotra,”A VLSI Architecture for Corner Detection,” Proc. Intl. Work. on Algorithms & Parallel VLSI Architectures, France, June 10-16, 1990.

199. N. Ranganathan, S. Subramanian and R. Mehrotra, ”A High Speed VLSI Architecture for Connected Component Labeling,” Proc. Intl. Workshop on Algorithms and Parallel VLSI Architectures, France, June 10-16, 1990.
200. N. Ranganathan and R. Mehrotra, ”A VLSI Based System for Motion Analysis in Scene Images,” Proc. IEEE Intl. Conf. on Tools for AI, Fairfax, VA, pp. 592-597, Oct 23-25, 1989.
201. A. Mukherjee, N. Ranganathan and M. Bassiouni,”Adaptive and Pipelined VLSI Designs for Treebased Codes,” Proc. IEEE Intl. Conf. on Computer Design (ICCD ’89), Cambridge, Massachusetts, pp. 369-373, Oct. 2-4, 1989.
202. A. Mukherjee, N. Ranganathan and M. Bassiouni, ”On Software and Hardware Techniques of Data Encoding,” Proc. of Fifth Intl. Conf. on Data Engineering, Los Angeles, pp. 208-215, Feb. 6-10, 1989.
203. N. Ranganathan and M. Shah, ”A Scale Space Chip,” Proceedings of 9th International Conference on Pattern Recognition, Roma, Italy, pp. 420-424, Nov. 14-18, 1988.
204. A. Mukherjee, N. Ranganathan and M. Bassiouni,”High Speed VLSI Encoding Chips for Supercomputers,” Proc. of 3rd Intl. Conf. on Supercomputing, Boston, May 15-20, 1988.
205. A. Mukherjee, M. Bassiouni and N. Ranganathan,”Improving Bandwidth of Communication Controllers,” Proc. of IEEE Intl. Conf. on Communications (ICC 88), Philadelphia, pp. 1390-1394, June 12-15, 1988.
206. M. Bassiouni, N. Ranganathan and A. Mukherjee, ”Software and Hardware Enhancement of Arithmetic Coding,” Proc. of 4th Int. Conf. on SSDBM, Roma, Italy, pp. 120-132, June 21-23, 1988.
207. M. Bassiouni, N. Ranganathan and A. Mukherjee,” A Scheme for Data Compression in Supercomputers,” Proc. of Supercomputing 88, Orlando, pp. 272-278, Nov. 14-18, 1988.

Invited Talks

1. ”Graduate Education in U.S. Universities”, Regional Engineering College, Tiruchi, July 1985.
2. ”Data Compression”, Indian Institute of Technology, Madras, India, June 1988.
3. ”Higher Education in Engineering”, St. Peter’s High School, Tanjore, Jun e 1988.
4. ”Data Compression Hardware”, IEEE and ACM Tampa Bay Section, October 1988.
5. ”VLSI Design”, Regional Engineering College, University of Madras, July 1989.
6. ”VLSI Algorithms and Architectures”, IIT-Madras and IEEE Madras Section, Dec 1990.
7. ”Performance in Very Large Databases”, K.J. Somaiya Institute, Bombay, Jan 1992.
8. ”VLSI for Data Compression,” University of Central Florida CS Colloquium, Sept. 23, 1992.
9. ”VLSI Hardware for Data Compression,” ACM/IEEE Tampa Bay Section, Nov 18, 1992.
10. Data Compression, East Tenn. State Uni. ACM chapter, Johnson City, TN, Nov 1993.
11. Data Compression, IIT, Bombay, IEEE DVP Speaker, Dec 1995.
12. VLSI For Pattern Matching, UCF, Orlando, April 1997.
13. Application Specific VLSI Systems, Uni. of Houston, April 1997.
14. Lossless Data Compression, ITEM University, Cuernavaca, October 1997.
15. Image Transmission over Wireless Channels, UCF, Orlando, IEEE DVP Speaker, Nov 1997.
16. Application Specific VLSI Systems, Uni. of Texas at El Paso, Feb 1998.
17. VLSI Systems for Data Compression, SVCE College of Eng., Uni. of Madras, May 1998.
18. Power Estimation and Optimization, Distinguished Speaker Lecture Series, Cadence Inc., Boston, September 2002.
19. ASICS as a Solution to Biomechanics, Invited Keynote address in Intl. Conf. on Biomechanics, April, 2004.
20. Impact of VLSI Technology on Future Computing, I2IT, Pune, India, Aug 2004.
21. Game Theoretic Optimization for Interconnect Design, Tata Consultancy Services, Bangalore, 2006.
22. Multimetric Optimization in VLSI CAD, Invited Keynote Address in Intl. Conf. on Brain Modeling and Supercomputing, 2007.
23. VLSI Technology and Its Future, Meenakshi College, Chennai, 2007.
24. Game Theory in VLSI CAD, Texas Instruments Bangalore, 2007.
25. Multimetric Challenges in Nanoscale Computer Design, USF University Lecture Series, 2007.
26. Invited Panel Speaker, VLSI Education in US Universities, Intl. Student Conf. on VLSI Design, hosted by VEDA-IIT, Hyderabad, 2008.
27. Multimetric Challenges in VLSI Design, EE Dept., IIT-Madras, 2008.
28. The Future of Computing Technology, Pontificia Catholic University, Lima, Peru, April 2009.
29. USF CSE Graduate Program Highlights, Pontificia Catholic University, Lima, Peru, April 2009.
30. Application Specific Architectures, KAIST, South Korea, May 2011.
31. Use of Game Theory in VLSI Design, KAIST, South Korea, May 2011.
32. Impact of VLSI Technology on Architecture, KAIST, South Korea, May 2011.

VLSI Chips Designed/Supervised

1. Design of an nMOS Pipeline Wallace Multiplier Chip, 1984.
2. Design of an nMOS chip for Polygonal Mask Generation, 1985.
3. Design of a Prototype CMOS Chip for Huffman-based Data Compression, 1987.
4. Design of a Systolic Array Processor Chip for Scale Space Computation, 1989.
5. Design of a Systolic Array CMOS Chip for LZ-based Data Compression, 1990.
6. Design of a Run-length Based Compression CMOS Chip, 1990.
7. Design of SIGMA: Systolic Chip for Galois Field-based Multiply/Divide, 1990.
8. Design of a Prototype CMOS Chip for Huffman-based Decompression, 1990.
9. Design of a Systolic CMOS Chip for Join Computation in RDBMS Systems, 1991.
10. Design of a Systolic Array Processor CMOS Chip for Dynamic Scene Analysis, 1991.
11. Design of a 2-D Systolic Array processor CMOS Chip for Image Processing, 1991.
12. Design of a Memory-based CMOS VLSI Chip for JPEG Baseline Compression, 1991.
13. Design of a CMOS VLSI Chip for Hierarchical Scene Matching, 1992.
14. Design of a CMOS VLSI Chip for Approximate String Matching, 1993.
15. Design of a CMOS VLSI Chip for Polygon Recognition, 1993.
16. Design of a CMOS VLSI Chip for Approximate Tree Matching, 1994.
17. Design of a CMOS VLSI Chip for Template Matching, 1994.
18. Design of a CMOS VLSI Chip for JPEG Image Compression Standard, 1994.
19. Design of a CMOS VLSI Chip for Image Thinning, 1995.
20. Design of a CMOS VLSI Chip for Tree Pattern Matching, 1995.
21. Design of a CMOS VLSI Chip for Intelligent Decision Making, 1995.
22. Design of a CMOS linear Array Processor with Variable Rate Clocking, 1995.
23. Design of a CMOS VLSI Chip for Maximal Matching in Bipartite Graphs, 1995.
24. Design of a Chip for Image Compression with Variable Size Segmentation, 1995.
25. Design of a Chip for Contiguous Binary String Matching CBS Problem, 1995.
26. Design of a CMOS VLSI Chip for Tree Matching, 1996.
27. Design of a CMOS Chip/FPGA board for Connected Component Labeling, 1996.
28. Design of a CMOS Chip for Cancer Detection using Digital Mammograms, 1996.
29. Design of a CMOS VLSI ATM Switch Prototype, 1997.
30. Design of a CMOS VLSI Chip for Motion Estimation from Video, 1998.
31. Design of a CMOS VLSI Chip for Object Recognition in Images, 2002.
32. Design of a CMOS VLSI Chip for Invisible Digital Image Watermarking, 2003.
33. Design of a CMOS VLSI Chip for Visible Digital Image Watermarking, 2003.
34. Design of a Dual Voltage-Frequency Chip for Watermarking in DCT Domain, 2004